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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,866	04/15/2004	Hakam D. Hussein	STL11730	7077

7590 12/26/2007  
Seagate Technology LLC  
1280 Disc Drive  
Shakopee, MN 55379

EXAMINER
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RUTLAND WALLIS, MICHAEL

ART UNIT	PAPER NUMBER
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2836

MAIL DATE	DELIVERY MODE
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12/26/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

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<b>Office Action Summary</b>	<b>Application No.</b>		<b>Applicant(s)</b>	
	10/824,866		HUSSEIN ET AL.	
	<b>Examiner</b>		<b>Art Unit</b>	
	Michael Rutland-Wallis		2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 12 November 2007.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☐ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Response to Arguments***

Applicant's arguments, filed 11/12/2007, with respect to the previous rejection of claims 1-25 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new grounds of rejection is made in view of Willis (U.S. Pat. No 6,225,797).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-8, 10-23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Willis (U.S. Pat. No 6,225,797)

With respect to claims 1, 13-15 and 19 Willis teaches an inrush current controller for a device (item 86 or 118), comprising (see Figs. 1 or 4): a connector (formed by interfacing circuitry connecting power source item 22 and device) for plugging the device into a source of energization (item 22), the connector including a first contact (item 38) for connecting to a first power supply contact of the source, a second contact

(item 94) for connecting to a logic output (item 46) from the source, and a third contact (for example item 40) for connecting to a second power supply contact of the source (22); an impedance (formed with the conduction control of item 24) having a current input that couples to a the first contact (38) of the connector, an impedance control input (32), and a current output (item 30) coupling to the device (26); and an impedance control circuit (item 50) having a logic input (via 46 and 94) coupling to a the second contact of the connector, and having an impedance control output (item 96) connected to the impedance control input (item 32), the impedance control output forcing the impedance OFF (high or isolation impedance, load and supply isolated) during a first time interval (time that load is off) controlled by a first timer (item 48), and the logic input output from the source enabling a limited inrush (intermediate level via item 54 see for example col. 7 lines 20-30) at the current input during a second time interval (time when item 24 is held partially on) controlled by a second timer (time constant associated with item 58 see col. 7 lines 55-60). Willis discloses only circuitry and a block diagram schematic of the system and does not illustrate the connector at level to show the details of the mating contacts. The inclusion of the contacts would have been obvious to one of ordinary skill in the art at the time of the invention to provide a secure connection to allow power to flow to the device and to program the control electronics shown in Willis.

With respect to claims 2 and 16 Willis teaches the device may be a computer or other electronic system (col. 4 lines 25-35) and the source of energization comprises a host system. Willis does not describe a data storage device or the host system is a

computer system. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Willis to further include the use of such a data storage device in order to provide power safety to sensitive computing equipment.

With respect to claims 3 and 20 Willis teaches the impedance may be continuously variable (see Fig. 3A) as a function of the control input.

With respect to claims 4, 17 and 21 Willis teaches the first timer couples to the current input and the impedance control output, and provides a first timer output that forces the impedance OFF (isolated impedance) during the first time interval; and an inrush current limit circuit (item 54) coupled to the logic input and the impedance control output, and providing an inrush current limit (rate of change of voltage ramp) output controlled by the second timer (58).

With respect to claims 5 and 22 Willis teaches the first timer (48) output overrides (col. 8 lines 1-15) the inrush current limit output (via item 30) to the impedance control output (see col. 9 lines 1-5).

With respect to claim 6 Willis is silent on the logic of the circuit as being open or closed after the first time interval. It would have been obvious to one of ordinary skill in the art at the time of the invention to use an open logic as a means to signal the expiration of the first time interval in order to control the impedance and limit inrush current.

With respect to claims 7 and 23 Willis teaches the inrush current limit output gradually changes the impedance control output during a turn-on interval so that a device voltage has a slew rate (see Fig. 3). Willis is silent on the range of 12 volts per

100 milliseconds, however It would have been obvious to one of ordinary skill in the art at the time of the invention to select components with such a time constant to operate with a slew rate of less than 12 volts per 100 milliseconds in order to protect sensitive devices from inrush currents.

With respect to claim 8 Willis teaches the device has impedance that is partially inductive.

With respect to claims 10, 18 and 25 Willis teaches the use of a first timer a while Willis is silent on the use of a transient signal to activate the timer. The timer disclosed in Willis is triggerable by a voltage signal supplied to the input including that of a transient signal. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Willis to use transient signal in order to activate the timer to quickly activate the timer.

With respect to claim 11 Willis teaches the logic input triggers the limited inrush when the logic input is open (isolated) circuit, and when the logic input is at a high level.

With respect to claim 12 Willis teaches the impedance comprises a transistor (item 24).

Claims 9 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Willis (U.S. Pat. No 6,225,797) in view of Ngo (U.S. Pat. No 6,525,515)

With respect to claims 9 and 24 Willis teaches the timer controllable, however does not teach the timer is automatically reset. Ngo teaches the timer resets automatically when the connector is disconnected from the source of energization (via startup timer and Auto-restart timer items 57 and 55). It would have been obvious to one

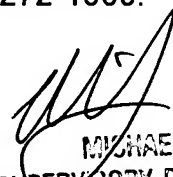
of ordinary skill in the art at the time of the invention to modify Willis to automatically reset in order to protect the device upon initial connection to the supply

### **Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Rutland-Wallis whose telephone number is 571-272-5921. The examiner can normally be reached on Monday-Thursday 7:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

 12/28/07  
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